CLAIMS

What is claimed is:

1. A method comprising;

placing one or more signal lines substantially between a match line and a data line in a CAM memory cell.

2. The method of claim 1 further comprising placing a second set of one or more signal lines substantially between said match line and a substantially inverted version of said data line in said CAM memory cell.

3. The method of claim 2 wherein said one or more signal lines and said second set of one or more signal lines are not the same signal lines.

4. The method of claim 2 wherein said one or more signal lines and said second set of one or more signal lines are selected from the group consisting of a positive voltage supply, a ground signal, a value bit, a data bit, a mask bit, a substantially inverted version of said value bit, a substantially inverted version of said data bit, and a substantially inverted version of said mask bit.

5. The method of claim 4 wherein said match line is selected from the group consisting of a low match line, and a high match line.

6. A method comprising:

not routing a match line of a negative exclusive OR (NXOR) circuit of a ternary CAM (TCAM) cell substantially parallel to a data line for said NXOR circuit.

7. The method of claim 6 further comprising:

not routing a match line of an NXOR circuit of a TCAM cell substantially parallel to a complement of said data line for said NXOR circuit.

8. A method comprising:

coupling less than all memory cells in a row of a sub-array of a CAM to a same sense amplifier;

coupling any remaining said less than all memory cells to a second sense amplifier and;

routing a data line substantially parallel to a match line, but not directly adjacent to said match line.

9. A method comprising:

coupling less than all memory cells in a row of a sub-array of a CAM to a first input of a multiple input sense amplifier;

coupling any remaining said less than all memory cells to one or more inputs other than said first input of said sense amplifier;

routing one or more signal lines between a low match line and a data line; and

routing one or more signal lines between said low match line and a complement of said data line.

10. The method of claim 9 wherein said multiple input sense amplifier is a two input sense amplifier.

11. The method of claim 10 wherein said one or more signal lines is selected from the group consisting of a voltage supply, a ground signal, a value bit, a data bit, a mask bit, a complement of said value bit, a complement of said data bit, and a complement of said mask bit.

12. A method for connecting cells in a row in a CAM sub-array, the method comprising:

separating a row match line into several submatch lines;

coupling less than all said cells in said row to a same sense amplifier; and

placing a trace between a low match line and a data line.

13. The method of claim 12 further comprising:

coupling any remaining said less than all said cells to one or more sense amplifiers; and

placing a trace between said low match line and a complement of said data line.

14. The method of claim 13 wherein said placing a trace is achieved using a substantially same set of interconnect layers.

15. The method of claim 13 wherein said placing a trace is achieved using a substantially different set of interconnect layers.

16. The method of claim 12 wherein said low match line and said data line are substantially parallel in routing.

17. A method for constructing an integrated circuit (IC) content addressable memory (CAM) comprising:

connecting less than all memory cells in a row of a sub-array of a CAM to a same sense amplifier;

connecting any remaining said less than all memory cells in said row of said sub-array of said CAM to a second sense amplifier; and

routing one or more signal lines between a match line and a compare data line and a complement of said compare data line associated with said memory cells in said row of said sub-array of said CAM.

18. The method of claim 17 wherein said connecting and routing uses a substantially different set of interconnect layers.

19. An apparatus comprising:

a plurality of memory cells arranged in a row;

one or more match lines running substantially parallel to said row;

means for connecting one or more said memory cells to said one or more match lines; and

one or more traces substantially parallel to and interspersed between said one or more match lines.

20. An apparatus comprising:

a plurality of memory cells arranged in a row;

one or more match lines running substantially parallel to said row;

means for connecting two or more subsets of said plurality of memory cells to said one or more match lines; and

one or more low match lines running substantially perpendicular to said row; and

one or more traces interspersed between said one or more low match lines and one or more data lines running substantially parallel to said one or more low match lines.

21. The apparatus of claim 20 wherein said plurality is a sub-array.

22. The apparatus of claim 20 wherein said one or more match lines connect to one or more sense amplifiers.

23. The apparatus of claim 20 wherein said one or more match lines connect to one or more inputs of a sense amplifier.

24. The apparatus of claim 20 wherein said means for connecting uses a substantially same set of integrated circuit interconnect layers.

25. The apparatus of claim 20 wherein said means for connecting uses a substantially different set of integrated circuit interconnect layers.

26. The apparatus of claim 20 wherein said means for connecting uses a same integrated circuit interconnect layer for a majority of distance of said one or more match lines.

27. The apparatus of claim 20 wherein said means for connecting uses a different integrated circuit interconnect layer for a majority of distance of said one or more match lines.

28. An apparatus comprising:

means for connecting memory cells in a row to two or more high match lines; and

means for routing a trace between a low match line and a data line.

29. The apparatus of claim 28 wherein less than all of said memory cells in said row are connected to a first high match line.

30. The apparatus of claim 29 wherein remaining less than all of said memory cells in said row are connected to one or more high match lines.

31. The apparatus of claim 30 further comprising:

an integrated circuit containing said memory cells in a row; and

said connection to said first high match line is through a substantially same set of integrated circuit interconnect layers as said connection to said one or more high match lines.

32. The apparatus of claim 31 further comprising said first high match line connected to a first amplifier and said one or more high match lines connected to one or more amplifiers.

33. The apparatus of claim 31 further comprising said first high match line connected to a first input of an N input amplifier and each said one or more high match lines connected to one or more inputs of said N input amplifier.

34. The apparatus of claim 32 wherein said connection to said first amplifier is through a substantially same set of integrated circuit interconnect layers as said connection to said one or more amplifiers.

35. The apparatus of claim 32 wherein said connection to said first amplifier is through a substantially different set of integrated circuit interconnect layers as said connection to said one or more amplifiers.

36. The apparatus of claim 30 further comprising:

an integrated circuit containing said memory cells in a row; and

said connection to said first high match line is through a substantially different set of integrated circuit interconnect layers as said connection to said one or more high match lines.

37. The apparatus of claim 36 further comprising said first high match line connected to a first amplifier and said one or more high match lines connected to one or more amplifiers.

38. The apparatus of claim 37 wherein said connection to said first amplifier is through a substantially same set of integrated circuit interconnect layers as said connection to said one or more amplifiers.

39. The apparatus of claim 37 wherein said connection to said first amplifier is through a substantially different set of integrated circuit interconnect layers as said connection to said one or more amplifiers.

40. A CAM comprising:

cells arranged in a row wherein less than all of said cells in said row are in communication with a single submatch line;

a first match line substantially parallel with said row and in communication with one or more said cells; and

a second match line in communication with one or more said cells.

41. The CAM of claim 40 further comprising one or more submatch lines in communication with any remaining cells not in communication with said single submatch line.

42. The CAM of claim 41 wherein a particular cell is in communication with a submatch line selected from the group consisting of said single submatch line, said one or more submatch lines, and any combination of said single submatch line and said one or more submatch lines.

43. The CAM of claim 41 further comprising a single sense amplifier coupled to receive input from said one or more submatch lines and said single submatch line.

44. The CAM of claim 41 further comprising a plurality of sense amplifiers coupled to receive input from a source selected from the group consisting of said one or more submatch lines, said single submatch line, and any combination of said one or more submatch lines and said single submatch line.

45. The CAM of claim 41 wherein said submatch lines are substantially of a same length.

46. The CAM of claim 41 wherein said submatch lines are of different lengths.

47. The CAM of claim 41 wherein said submatch lines use substantially the same IC interconnect layers.

48. The CAM of claim 41 wherein said submatch lines use different IC interconnect layers.

49. The CAM of claim 41 wherein said submatch lines are substantially of a same capacitance.

50. The CAM of claim 41 wherein a particular cell is in communication with said one or more submatch lines and said single submatch line.

51. A machine-readable medium having stored thereon information representing the apparatus of claim 40.

52. An apparatus comprising:

a value memory cell for storing a data value;

a value word line capable of allowing communication of said value memory cell with one or more value data lines;

a mask memory cell for storing a mask value;

a mask word line capable of allowing communication of said value mask memory cell with one or more mask data lines; and

a NXOR comparison circuit having a high match line, a low match line, and inputs, said inputs in communication with said data value, said mask value, and one or more compare data lines.

53. The apparatus of claim of 52 wherein said value word line and said mask word line are

the same line.

54. The apparatus of claim 52 wherein said low match line runs substantially parallel with said one or more compare data lines.

55. The apparatus of claim 54 wherein said low match line and said one or more compare lines are not directly adjacent.

56. The apparatus of claim 54 wherein there are one or more traces running substantially parallel with said low match line and said one or more traces are located between said low match line and said one or more data compare lines.

57. A method comprising;

placing one or more lines substantially between a match line pickup via and a data line in a CAM memory cell.

58. The method of claim 57 further comprising placing a second set of one or more lines substantially between said match line pickup via and a substantially inverted version of said data line in said CAM memory cell.

59. The method of claim 58 wherein said one or more lines and said second set of one or more lines are not the same lines.

60. The method of claim 58 wherein said one or more lines and said second set of one or more lines are selected from the group consisting of a voltage supply, a ground, a value bit, a data bit, a mask bit, a substantially inverted version of said value bit, a substantially inverted version of said data bit, a substantially inverted version of said mask bit, a word line, a bypass line, and a signal line.

61. The method of claim 60 wherein said match line pickup via is selected from the group consisting of a low match line pickup via, and a high match line pickup via.

62. A method comprising:

coupling less than all memory cells in a row of a sub-array of a CAM to a same sense amplifier;

coupling any remaining said less than all memory cells to a second sense amplifier and;

routing one or more lines between a data line and a match line via.

63. A method comprising:

coupling less than all memory cells in a row of a sub-array of a CAM to a first input of a multiple input sense amplifier;

coupling any remaining said less than all memory cells to one or more inputs other than said first input of said sense amplifier;

routing one or more lines between a low match line pickup via and a data line; and

routing one or more lines between said low match line and a complement of said

data line.

64. The method of claim 63 wherein said multiple input sense amplifier is a two input sense amplifier.

65. The method of claim 64 wherein said one or more lines is selected from the group consisting of a voltage supply, a ground signal, a value bit, a data bit, a mask bit, a complement of said value bit, a complement of said data bit, and a complement of said mask bit.

66. A method for connecting cells in a row in a CAM sub-array, the method comprising:

separating a row match line into several submatch lines;

coupling less than all said cells in said row to a same sense amplifier; and

placing a trace between a match line pickup via and a data line.

67. A method for constructing an integrated circuit (IC) content addressable memory (CAM) comprising:

connecting less than all memory cells in a row of a sub-array of a CAM to a same sense amplifier;

connecting any remaining said less than all memory cells in said row of said sub-array of said CAM to a second sense amplifier; and

routing one or more signal lines between a match line pickup via and a compare data line and a complement of said compare data line associated with said memory cells in

said row of said sub-array of said CAM.

68. An apparatus comprising:

a plurality of memory cells arranged in a row;

one or more match lines running substantially parallel to said row;

vias for connecting one or more said memory cells to said one or more match lines; and

one or more traces between said vias and data lines.

69. An apparatus comprising:

via means for connecting memory cells in a row to two or more match lines; and

means for routing a trace between said via means and one or more data lines.

70. The apparatus of claim 69 wherein less than all of said memory cells in said row are connected to a first match line.

71. The apparatus of claim 70 wherein remaining less than all of said memory cells in said row are connected to one or more match lines.

72. An apparatus comprising:

a value memory cell for storing a data value;

a value word line capable of allowing communication of said value memory cell with one or more value data lines;

a mask memory cell for storing a mask value;

a mask word line capable of allowing communication of said value mask memory cell with one or more mask data lines;

a comparison circuit having a match line, and inputs, said inputs in communication with said data value, said mask value, and one or more compare data lines; and

a connection to said match line separated from said one or more compare data lines by one or more lines selected from the group consisting of said value word line, said one or more value data lines, said mask word line, a power supply line, a ground line, and one or more match lines other than said match line.

73. The apparatus of claim 72 wherein said connection to said match line is a via.

74. The apparatus of claim of 72 wherein said value word line and said mask word line are the same line.

75. A method for reducing cross-coupling between a match line via and a data line, the method comprising:

routing one or more lines between said match line via and said data line.

76. The method of claim 75 wherein said one or more lines are on a substantially same layer as said data line.

77. A method for reducing cross-coupling between a data line via and a match line, the method comprising:

routing one or more lines between said data line via and said match line.

78. The method of claim 77 wherein said one or more lines are on substantially a same layer as said match line.

79. A method for reducing cross-coupling between a data line and a match line that are substantially parallel, the method comprising:

routing one or more lines between a data line via and said match line.

80. The method of claim 79 wherein said one or more lines are on substantially a layer selected from the group consisting of a same layer as said data line, a same layer as said match line, one or more layers substantially between said data line and said match line.

81. A method for reducing cross-coupling between a via and a line that are on substantially a same layer, the method comprising:

routing one or more lines between said via and said line.

82. A method for reducing cross-coupling between a first via and a second via, the method comprising:

routing one or more lines between said first via and said second via.

83. The method of claim 82 wherein said one or more lines are on substantially a layer selected from the group consisting of a same layer as said first via, a same layer as said second via, one or more layers substantially between said first via and said second via.

84. The method of claim 83 wherein said first via is a data line via and said second via is a match line via.

85. A method for connecting cells in a row in a CAM sub-array, the method comprising:

separating a row match line into several submatch lines;

coupling less than all said cells in said row to a same sense amplifier; and

placing a trace between a data line pickup via and a match line.

86. An apparatus comprising:

a plurality of memory cells arranged in a row;

one or more data lines running substantially perpendicular to said row;

vias for connecting one or more said memory cells to said one or more data lines; and

one or more traces between said vias and match lines.

87. An apparatus comprising:

via means for connecting memory cells in a row to data lines; and

means for routing a trace between said via means and one or more match lines.